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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,066	ROTH ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-26,28,29 and 31-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-26,28,29 and 31-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-26, 28, 29, 31-34, and 36-39 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Alidina et al., US Patent 5,991,785.

3. Referring to claim 1, Alidina et al. have taught a method comprising:

a. receiving N/M machine instructions directing a processor to search an array of N data elements, where N and M are integers greater than one (column 4, lines 22-44); and

b. executing a first machine instruction by concurrently comparing M data elements retrieved when executing a previous machine instruction to M corresponding current extreme values (column 4, line 22-column 5, line 44, a0 and a2 are concurrently compared with a1 and a3. The DSP16000 architecture is pipelined. The fetch stage is separate from the execution stage. Therefore the data is retrieved when executing a previous machine instruction.);

c. updating a set of M references based on said comparing (column 4, line 22-column 5, line 44); and

d. retrieving another M elements in a single fetch cycle to be compared when executing a subsequent machine instruction (column 5, lines 1-15, The DSP 16000

architecture is pipelined. In pipelined systems, while instructions are being executed, new instructions are fetched. Therefore, when this claimed instruction is being executed, a new instruction is fetched.).

4. Referring to claim 2, Alidina et al. have taught the method of claim 1, as described above, and wherein said retrieving another M data elements comprises retrieving the another M data elements as a single data quantity containing the another M data elements (column 4, line 55-column 5, line 54).

5. Referring to claim 3, Alidina et al. have taught the method of claim 2, as described above, and wherein the set of M references comprise pointer registers to store addresses of extreme data quantities in the array of N data elements (column 4, line 22-column 5, line 44).

6. Referring to claim 5, Alidina et al. have taught the method of claim 1, as described above, and where M=2 and N is great that two (column 4, line 22-column 5, line 44).

7. Referring to claim 6, Alidina et al. have taught the method of claim 1, as described above, and wherein executing the first machine instruction further includes:

a. storing the current M extreme values in M accumulators (column 4, lines 44-67); and

b. copying the M data elements to the accumulators based on said comparing (column 4, line 22-column 5, line 44).

8. Referring to claim 7, Alidina et al. have taught the method of claim 5, as described above, and wherein said concurrently comparing the M data elements comprises processing a fist data element with a first execution unit of a pipelines processor (column 3, lines 15-22, column 4

lines 34-44) and processing a second data element with a second execution unit of the pipelined processor (column 3, lines 15-22, column 4 lines 34-44).

9. Referring to claim 8, Alidina et al. have taught the method of claim 5, as described above, and wherein concurrently comparing the M data elements comprises concurrently processing a first data element and a second data element within a single execution unit of a pipelined processor (Figure 1, "ADDER" or "ALU/ACS").

10. Referring to claim 9, Alidina et al. have taught the method of claim 1, as described above, and wherein said concurrently comparing the M data elements to M corresponding current extreme values includes determining whether each of the data elements is less that the corresponding current extreme value (column 4, line 22-column 5, line 44).

11. Referring to claim 10, Alidina et al. have taught the method of claim 1, as described above, and wherein said concurrently comparing the M data elements to M corresponding current extreme values includes determining whether each of the data elements is greater than the corresponding current extreme values (column 4, line 22-column 5, line 44).

12. Referring to claim 11, Alidina et al. have taught a method for searching an array of N data elements for an extreme value, the method comprising:

a. issuing N/M machine instructions to a processor, wherein the processor is adapted to process M data elements in parallel (column 4, lines 22-44);

13. b. executing each machine instruction by:

c. concurrently comparing M data elements to corresponding M current extreme values (column 4, line 22-column 5, line 44, a0 and a2 are concurrently compared with a1 and a3.),

d. retrieving another M elements in a single fetch cycle to be compared when executing a subsequent machine instruction (column 5, lines 1-15, The DSP 16000 architecture is pipelined. In pipelined systems, while instructions are being executed, new instructions are fetched. Therefore, when this claimed instruction is being executed, a new instruction is fetched., or retrieved);

e. updating accumulators and pointers associated with the M current extreme values based on said comparing, and analyzing results of the machine instructions to identify at least a value and a position of at least one extreme value in the array (column 4, line 22-column 5, line 44).

14. Referring to claim 12, Alidina et al. have taught the method of claim 11, as described above, and further comprising:

a. setting up registers for said accumulators and pointers (column 4, lines 23-33, MIN_VALUE and MIN_INDEX).

15. Referring to claim 13, Alidina et al. have taught a method comprising retrieving a pair of data elements from an array of elements in a single fetch operation, wherein the pair of data elements includes an even data element and an odd data element (column 4, line 44-column 5, line 12);

a. substantially comparing the even element of the pair with an even extreme value (column 4, line 22-column 5, line 44);

b. if the even element of the pair exceeds the even extreme value, storing the even element of the pair as the even extreme value and storing a parameter indicative of a location of the even element of the pair (column 4, line 44-column 5, line 12);

c. concurrent with said comparing the even element of the pair with the even extreme value, comparing the odd element of the pair with an odd extreme value (column 4, line 44-column 5, line 12);

d. if the odd element of the pair exceeds the odd extreme value, storing the odd element of the pair as the odd extreme value (column 4, line 44-column 5, line 12); and

e. substantially fetching and comparing the remaining pairs of data elements of the array until all of the data elements of the array have been processed (column 4, line 44-column 5, line 12).

16. Referring to claim 14, Alidina et al. have taught the method of claim 13, as described above, and further comprises setting the even extreme value as a function of the even element of the element pair and setting the odd extreme value as a function of the odd element of the pair (column 4, line 22-column 5, line 44).

17. Referring to claim 15, Alidina et al. have taught the method of claim 13, as described above, and further comprises maintaining a first accumulator to store a minimum value for the even elements (column 4, lines 44-52, a2) and a second accumulator to store a minimum value of the odd elements (column 4, lines 44-52, a3).

18. Referring to claim 16, Alidina et al. have taught the method of claim 13, as described above, and wherein storing the parameter indicative of a location of the even element of the pair comprises maintaining a first pointer register to store an address for the extreme value of the even data elements (column 4, lines 22-33, column 6, lines 30-39), and further comprising maintaining a second pointer register to store an address for the extreme value of the odd data elements (column 4, lines 22-33, column 6, lines 30-39).

19. Referring to claim 17, Alidina et al. have taught the method of claim 16, as described above, and further including adjusting at least one of the pointer registers after processing all of the pairs of data elements to account for a number of stages in a pipeline (column 5, lines 1-12, after comparing all of the pairs of data, the two running extrema are compared, to account for all of the stages in the pipeline.).

20. Referring to claim 18, Alidina et al. have taught the method of claim 13, as described above, and wherein the method is invoked by issuing N/M machine instructions to a programmable processor, wherein N equals a number of elements in the array, and M equals a number of data elements that the processor can concurrently compare (column 4, line 22-column 5, line 44, 2 and n=N)

21. Claim 19 does not claim anything over claim 11 and is therefore rejected for the same reasons as claim 11.

22. Claim 20 does not claim anything over claim 12 and is therefore rejected for the same reasons as claim 12.

23. Claim 21 does not claim anything over claims 11 and 12 and is therefore rejected for the same reasons as claims 11 and 12.

24. Claim 22 does not claim anything over claim 3 and is therefore rejected for the same reasons as claim 3.

25. Referring to claim 23, Alidina et al. have taught the apparatus of claim 21, as described above, and wherein the registers are general-purpose registers (column 4, lines 44-52)

26. Referring to claim 24, Alidina et al. have taught the apparatus of claim 19, as described above, and wherein the pipeline includes M accumulators to store M current extreme values (column 4, lines 44-52).

27. Referring to claim 25, Alidina et al. have taught the apparatus of claim 19, as described above, and wherein the pipeline includes M general-purpose registers to store M current extreme values (column 4, lines 44-52).

28. Claim 26 does not claim anything over claim 12 and is therefore rejected for the same reasons as claim 12.

29. Claim 28 does not claim anything over claim 8 and is therefore rejected for the same reasons as claim 8.

30. Referring to claim 29, Alidina et al. have taught a system comprising:

a. a memory device (column 1, lines 12-19); and

b. a processor coupled to the memory device (column 2, lines 59-65), wherein the processor includes a pipeline configured to process M data elements in parallel (column 4, line 22-column 5, line 44, where M=2) and a control unit configured to direct the pipeline to search an array of N data elements for an extreme value in response to N/M machine instruction, wherein in response to each of the machine instructions (column 4, line 22-column 5, line 44), the pipeline being configured to:

i. retrieve M data elements from the array of N data elements in a single fetch cycle (column 4, line 44-column 5, line 12);

ii. concurrently compare the retrieved M data elements to corresponding M current extrmeme values (column 4, line 44-column 5, line 12), and

iii. update accumulators and pointers associated with the M current extreme values based on said comparing (column 4, line 44-column 5, line 12).

31. Referring to claim 31, Alidina et al. have taught the system of claim 29, as described above, and wherein the pipeline includes M registers configured to store the accumulators and pointers (column 4, lines 22-52).

32. Referring to claim 32, Alidina et al. have taught the system of claim 31, as described above, and wherein the registers are pointer registers (column 4, lines 22-52, MIN_INDEX).

33. Referring to claim 33, Alidina et al. have taught the system of claim 31, as described above, and wherein the registers are general-purpose data registers (column 4, lines 22-52).

34. Referring to claim 34, The system of claim 29, wherein the memory device comprises static random access memory (column 1, lines 12-19).

35. Referring to claim 36, Alidina et al. have taught the method of claim 11, as described above, and wherein the at least a value and a position of the at least one extreme value in the array comprises a value and a position of a first occurrence of a minimum value in the array (column 4, line 22-column 5, line 44, MIN_VALUE, MIN_INDEX).

36. Referring to claim 37, Alidina et al. have taught the method of claim 11, as described above, and wherein the at least a value and a position of at least one extreme value in the array comprises a value and a position of a last occurrence of a minimum value in the array (column 4, line 22-column 5, line 44).

37. Referring to claim 38, Alidina et al. have taught the method of claim 11, as described above, and wherein the at least a value and a position of at least one extreme value in the array

comprises a value and a position of a last occurrence of a maximum value in the array (column 4, line 22-column 5, line 44).

38. Referring to claim 39, Alidina et al. have taught the method of claim 11, as described above, and wherein the at least a value and a position of at least one extreme value in the array comprises a value and a position of a first occurrence of a maximum value in the array (column 4, line 22-column 5, line 44).

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al., US Patent 5,991,785. Alidina et al. have taught the system of claim 29, as described above.

41. While Alidina et al. may not have taught wherein the memory device comprises FLASH memory, it is well known that flash memory is connected to processors for the purpose of providing nonvolatile memory to maintain data between sessions. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Alidina et al. include a flash memory connected to the processor for the desirable purpose of providing nonvolatile memory to maintain data between sessions.

Response to Arguments

42. Applicant's arguments with respect to claims 1-3, 5-26, 28, 29, 31-35-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

44. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

45. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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